

SPICE Device Model SUM23N15-73

Vishay Siliconix

N-Channel 150-V (D-S), 175°C MOSFET

CHARACTERISTICS

- N-Channel Vertical DMOS
- · Macro Model (Subcircuit Model)
- Level 3 MOS

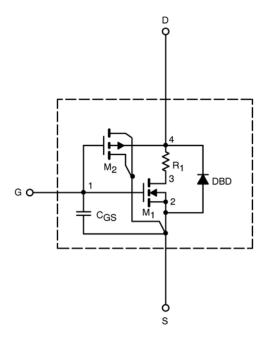
- Apply for both Linear and Switching Application
- Accurate over the -55 to 125°C Temperature Range
- Model the Gate Charge, Transient, and Diode Reverse Recovery Characteristics

DESCRIPTION

The attached spice model describes the typical electrical characteristics of the n-channel vertical DMOS. The subcircuit model is extracted and optimized over the -55 to 125° C temperature ranges under the pulsed 0-V to 10-V gate drive. The saturated output impedance is best fit at the gate bias near the threshold voltage.

A novel gate-to-drain feedback capacitance network is used to model the gate charge characteristics while avoiding convergence difficulties of the switched $C_{\rm gd}$ model. All model parameter values are optimized to provide a best fit to the measured electrical data and are not intended as an exact physical interpretation of the device.

SUBCIRCUIT MODEL SCHEMATIC



This document is intended as a SPICE modeling guideline and does not constitute a commercial product data sheet. Designers should refer to the appropriate data sheet of the same number for guaranteed specification limits.

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SPECIFICATIONS (T _J = 25°C UNLESS OTHERWISE NOTED)					
Parameter	Symbol	Test Condition	Simulated Data	Measured Data	Unit
Static	· ·		-		
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_{D} = 250 \mu A$	3		V
On-State Drain Current ^a	I _{D(on)}	$V_{DS} \ge 5 \text{ V}, V_{GS} = 10 \text{ V}$	84		Α
Drain-Source On-State Resistance ^a	r _{DS(on)}	V _{GS} = 10 V, I _D = 15 A	0.059	0.059	Ω
		V _{GS} = 10 V, I _D = 15 A, T _J = 125°C	0.011		
		V _{GS} = 10 V, I _D = 15 A, T _J = 175°C	0.134		
		V _{GS} = 6 V, I _D = 10 A	0.064	0.062	
Forward Voltage ^a	V_{SD}	I _F = 23 A, V _{GS} = 0 V	0.89	1	V
Dynamic ^b					
Input Capacitance	C_{iss}	V _{GS} = 0 V, V _{DS} = 25 V, f = 1 MHz	1290	1290	pF
Output Capacitance	Coss		150	160	
Reverse Transfer Capacitance	C_{rss}		60	70	
Total Gate Charge ^c	Q_g	V_{DS} = 75 V, V_{GS} = 10 V, I_{D} = 23 A	22	22	nC
Gate-Source Charge ^c	Q_{gs}		6	6	
Gate-Drain Charge ^c	Q_{gd}		7.5	7.5	
Turn-On Delay Time ^c	t _{d(on)}	$V_{DD} = 75 \text{ V}, R_L = 3.26 \Omega$ $I_D \cong 23 A, V_{GEN} = 10 \text{ V}, R_G = 2.5 \Omega$	37	10	ns
Rise Time ^c	t _r		29	60	
Turn-Off Delay Time ^c	t _{d(off)}		29	30	
Fall Time ^c	t _f		12	45	

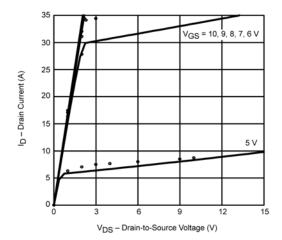
- Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2%. Guaranteed by design, not subject to production testing. Independent of operating temperature.

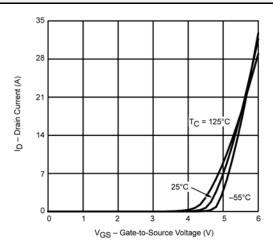


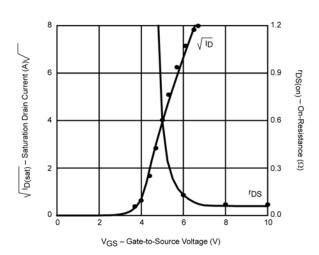
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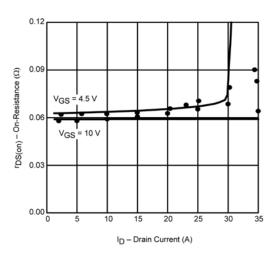
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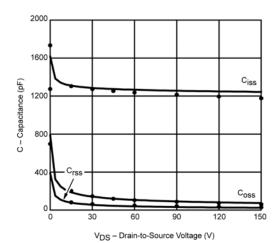
COMPARISON OF MODEL WITH MEASURED DATA (TJ=25°C UNLESS OTHERWISE NOTED)

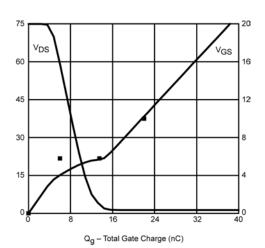












Note: Dots and squares represent measured data.



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